REMARKS/ARGUMENTS

Claims 1-19 are now pending. Claims 1, 5, 6, 9, 10, 11, 12, 15, 16, and 19 have been amended. No new matter has been introduced.

In the Office Action, the Examiner noted certain informalities in the specification. Applicants have corrected the specification to correct the inadvertently introduced typographical errors. Figure 9 is objected to as failing to comply with 37 CFR 1.84(p)(5) because it includes the reference characters (903) not mention in the description. Accordingly, Applicants have corrected the specification to include the omitted reference characters. Applicants respectfully request Examiner reconsider and withdraw objections to Figure 9 in light of the amended specification.

As noted, Applicants have amended claim 1 to clarify the present invention to overcome the Examiner's rejection under 35 U.S.C. §102(b) as being anticipated by Cho et al.(U. S. Patent No 6,242,332). Applicants have also amended claim 11 to further clarify the present invention to overcome the Examiner's rejection under 35 U.S.C §103(a) as unpatentable over Cho et al. in view of Jin et al. (U.S. Patent No 6,576,963). As clearly noted, the cited references, alone or in combination, fail to suggest or disclose each of the features of the present method for fabricating DRAM gate structures as claimed. The method includes forming a first gate structure and a second gate structure overlying the substrate. The first gate structure and the second gate structure each includes an overlying cap structure. Nowhere in the cited references show or suggest a gate structure including an overlying cap structure as recited in claim 1, as amended.

The method also includes performing a second etching process to remove a portion of the conformal dielectric layer on the bit line region, a portion of the conformal dielectric layer on the capacitor contact region while using other portions of the conformal dielectric layer and each of the caps as a mask to prevent the first gate structure and the second gate structure to be exposed as recited by claim 1. In contrast, shown in Figure 3G, as well as in Figure 6A, the etching process suggested by Cho et al. removes the conformal dielectric 118 entirely in the continuous common region. The conforming dielectric suggested by Cho et al. is not used as a mask to prevent the gate structures to be exposed as claimed. The etching process

suggested by Cho et al. also removes a portion of the side wall spacer, exposing the dielectric layers 110 and 112. Accordingly, Cho et al. fails to show or suggest the second etching process to remove a portion of the conformal dielectric layer on the bit line region, a portion of the conformal dielectric layer on the capacitor contact region while using other portions of the conformal dielectric layer and each of the caps as a mask to prevent the first gate structure and the second gate structure to be exposed as recited by claim 1.

Claim 1 recites also in part polysilicon is deposited within the continuous common region and overlying the bit line region, the capacitor contact region, the first gate structure, and the second gate structure The polysilicon and a portion of the interlayer dielectric are planarized exposing a portion of the first gate structure and a portion of the second gate structure leaving a portion of the polysilicon on the bit line region and the capacitor contact region. The polysilicon on the portion of the bit line region is isolated from the polysilicon on the portion of the capacitor contact region. Cho et al., again, fails to show or suggest these claimed features. Cho et al., shown in Figure 3H and Figure 6C, planarization of the polysilicon conductive layer 122. Figure 3H shows silicon oxide 110 and silicon nitride 112 remain and in Figure 6C, silicon oxide 110 remains overlying the gate structures. The gate structures suggested in Cho et al. are isolated by the oxide/nitride layer or the oxide layer remained, which is contrary to those elements recited by the claimed invention. Accordingly, claim1 is patentable over the cited references. Claims 2-10, as well as additional features therein, which depend upon claim 1 should be patentable at least for the reasons noted.

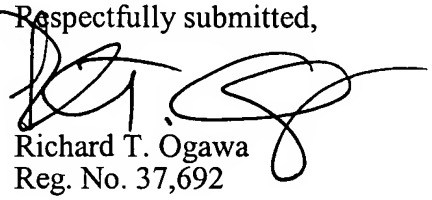
To cure the deficiencies of Cho, et al., the Examiner has cited Jin et al. to allegedly show that the method of forming self aligned contact holes being applied not only to a cell area but may be applied to the periphery circuit does not remove the aforementioned deficiencies in Cho et al. Based upon the amendments to the present specification, Jin et al. is irrelevant. Even if combined with Cho, et al., they fail to show or suggest the inventions of claims 1 and 11. Accordingly claim 11 is patentable over the cited references for a similar rationale as discussed for claim 1. Claims 12-19 which depend upon claim 11 should also be allowed for the reasons noted. Accordingly, all claims are patentable for at least these reasons and others.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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